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METHOD FOR TREATING SEMICONDUCTOR PROCESSING COMPONENTS AND COMPONENTS FORMED THEREBY

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CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application is a continuation-in-part application of US 10/414,563, filed April 15, 2003, and claims priority thereto under 35 USC 120.

BACKGROUND

Field of the Invention

[0002] The present invention is generally related to methods for treating semiconductor processing components for use in a semiconductor fabrication environment, as well as semiconductor processing components formed thereby.

Description of the Related Art

[0003] In the art of semiconductor processing, typically integrated circuit devices are formed through various wafer processing techniques, in which semiconductor (principally silicon) wafers are processed through various stations or tools. Processing operations include, for example, high temperature diffusion, thermal processing, ion implant, annealing, photolithography, polishing, deposition, etc. As new generation semiconductor devices are developed, an intense demand continues to exist in the industry to achieve better purity levels during such processing operations. In addition, there continues to be an intense driving force in transitioning to larger semiconductor wafers. Currently, the semiconductor industry is undergoing a transition from 200mm to 300mm wafers. The desire for superior purity levels and larger wafers introduces further integration challenges for next generation processing.

[0004] U.S. Patent 6,093,644 discloses a process in which an oxidation step is carried out, followed by oxide layer removal. However, the techniques disclosed therein do not adequately address certain contamination issues, and appear to focus on global impurity levels of the component, and not impurity levels along critical portions of the component. Further, the technology appears limited to restoring pre-machined purity levels to the component in the post-machined state.

[0005] Despite improvements in the industry to address next generation purity concerns as well as handling issues associated with larger-sized semiconductor wafers, a need continues to exist in the art for further improved semiconductor processing components, methods for forming such components, and methods for processing semiconductor wafers.

SUMMARY

[0006] According to one aspect of the invention, a semiconductor processing component is provided, the component comprising silicon carbide, wherein an outer surface portion of the component has a surface impurity level and a bulk impurity level. Preferably, the surface impurity level is not greater than ten times the bulk impurity level.

[0007] According to another embodiment, a method for treating a semiconductor processing component is provided. The method begins with provision of a semiconductor processing component having an outer surface portion formed by chemical vapor deposition of silicon carbide, the outer surface portion having a bulk impurity level and a surface impurity level. Further, a target portion of the outer surface portion is removed, such that the surface impurity level is not greater than about ten times the bulk impurity level.

[0008] Still further, according to another embodiment, a method for treating a semiconductor processing component is provided. The method begins with provision of a semiconductor processing component having an outer surface portion formed by chemical vapor deposition of silicon carbide. The outer surface portion has a bulk impurity level and a surface impurity level. Further, the method continues with removal

of a target portion of the outer surface portion, such that the surface impurity level is reduced by a factor of at least ten.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present invention may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0010] FIG. 1 illustrates an embodiment of the present invention, namely a wafer boat or carrier.

[0011] FIGS. 2 and 3 illustrate the impurity depth profile of CVD-SiC films formed in two different commercially available deposition apparatuses.

[0012] FIG. 4 illustrates the impurity depth profile of CVD-SiC, formed utilizing reactant gases at higher contaminant levels.

[0013] FIG. 5 illustrates the impurity depth profile of a CVD-SiC layer before and after an initial cleaning step.

[0014] FIG. 6 illustrates a depth profile resulting from two cleaning cycles of another sample, having a relatively low-purity CVD-SiC layer.

[0015] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[0016] According to aspects of the present invention, a semiconductor processing component, and a method for treating a semiconductor processing component are provided. The semiconductor processing component generally is formed at least partially of SiC, including an outer surface portion that has a controlled impurity content. The

outer surface portion is typically formed by chemical vapor deposition (CVD), and has an outer purity that is not greater than ten times a bulk purity. The outer surface portion may be defined as an identifiable SiC layer formed by CVD, or an outer thickness of a SiC component formed principally by CVD, as in the case of free-standing CVD-SiC components, described in more detail below.

[0017] According to one aspect, the present inventors have recognized that as-deposited CVD-SiC has a spike in impurity levels at the outer surface thereof, typically within the first 0.5 μm, such as within the first 0.25 μm, or the first 0.10 μm of the outer depth of the component. While, in contrast, the impurity level through the bulk of the outer surface portion stabilizes at a relatively low level, oftentimes one, two, or even three orders of magnitude lower than an impurity level at the very outer surface of the component. The bulk impurity level is generally that impurity level which represents the constant or nominal impurity level as a function of depth, and is further described hereinbelow. The foregoing a phenomenon is generally not recognized in the art, and rigorous analysis of as-deposited CVD-SiC layers has revealed a significant spread in impurity levels. Impurity levels are generally based on at least one of or a combination of Cr, Fe, Cu, Ni Al, Ca, Na, Zn, and Ti concentrations, between the outer surface and the bulk portion of the outer surface portion. According to an embodiment, the impurity levels are based on one of or both Fe and Cr.

[0018] In this context, according to another embodiment of the present invention, a semiconductor processing component having an outer surface portion formed by chemical vapor deposition of SiC is provided, and a target portion of the outer surface portion is removed, such that a surface impurity level of the outer surface portion is not greater than about ten times the bulk impurity level of the outer surface portion. While a maximum 10X difference in impurity levels between the bulk and the surface is generally desired, further embodiments have a surface impurity level that is not greater than about five times, such as not greater than about two times the bulk impurity level. Indeed, certain embodiments have a surface impurity level that is not greater than the bulk impurity level.

[0019] The semiconductor processing component according to embodiments herein may be chosen from one of various geometric configurations for different processing operations, and may be configured for receiving various sized wafers, whether 150mm, 200mm, or newer generation 300mm wafers, for example. Particular processing components include semiconductor wafer paddles, process tubes, wafer boats, liners, pedestals, long boats, cantilever rods, wafer carriers, vertical process chambers, and even dummy wafers. Of the foregoing, several of the semiconductor processing components may be those that are configured for direct contact with and for receiving semiconductor wafers such as horizontal or vertical wafer boats, long boats, and wafer susceptors. In addition, the processing component may be configured for single wafer processing and may be used for chambers, focus rings, suspension rings, susceptors, pedestals, etc.

[0020] The semiconductor processing component may be fabricated by various techniques. For example, according to one embodiment, the processing component is formed by provision of a substrate that is generally coated with a SiC layer by CVD. The CVD-SiC layer may advantageously function to attenuate auto-doping of the underlying silicon, as well as prevent migration of impurities from the bulk of the substrate to an outer surface of the component, which may lead to contamination during semiconductor wafer processing. The substrate typically functions to provide mechanical support and structural integrity, and may be formed of various materials, such as recrystallized SiC, and by various processing pathways. In one technique, the substrate, primarily composed of SiC, is formed by slip casting or by pressing. In the case of slip casting, the slip-cast body is dried and heat treated, followed optionally by impregnation to reduce porosity. Advantageously, impregnation may be carried out by infiltration with molten silicon. Other specialized fabrication techniques may also be used, such as by utilizing a conversion process in which a carbon preform is converted into a silicon carbide core, or by subtractive process in which the core is removed following infiltration, such as by chemical vapor infiltration.

[0021] Alternatively, the semiconductor processing component may be formed of stand-alone silicon carbide, formed of one of various processes such as by CVD of silicon carbide. This particular process technique enables formation of a processing component

that is of relatively high purity throughout substantially the entire bulk or interior portion of the component.

[0022] An embodiment of a wafer processing component is shown in FIG. 1. Wafer boat 1 illustrated in FIG. 1 has a plurality of grooves 16, each of which extends along the same radius of curvature. Each groove has an individual groove segment 18, 20 and 22, which are desirably machined following fabrication of the wafer boat proper. For example, the wafer boat may be fabricated according to one of the techniques described above, such as by impregnating a silicon carbide core with molten elemental silicon, then executing CVD to form a deposited silicon carbide layer. Following formation of the silicon carbide layer, machining may be carried out. In particular, the grooves may be formed and fine dimensional control may be executed by a machining operation, such as by utilizing a diamond-based machining tool. Noteworthy, while FIG. 1 illustrates a horizontal wafer boat, it is to be understood that vertical wafer boats or wafer carriers may be utilized as well, as well as other semiconductor processing components as already mentioned.

[0023] Following formation of the processing component, the processing component is subjected to a treatment process. Namely, the outer portion of the component formed of CVD-SiC is manipulated to improve purity, and particularly, the impurity of the outer surface. In one embodiment, a target portion of the outer surface portion is removed, leaving behind an outer surface that has an impurity content that is not greater than ten times that of a bulk impurity content of the outer surface portion.

[0024] Removal of the target portion may be carried out by any one of several techniques. According to one technique, the outer surface portion is removed by an oxidation-stripping process. During oxidation, the component may be exposed to a reactant species, such as a halogen gas, to further improve purity. The reactant species generally functions to complex or react with existing impurities, and volatilize during high temperature treatment. Oxidation-stripping may also reduce particle count along the outer surface, particularly beneficial in the context of semiconductor processing operations.

[0025] In more detail, oxidation of the semiconductor processing component is generally carried out to form an oxide layer by chemical reaction to form a conversion layer, as opposed to a deposited oxide layer. According to the oxidation treatment, an oxide layer consumes a target portion of the component, namely a portion of the CVD-SiC material. The oxide layer may be formed by oxidation of the component in an oxidizing environment, such as by oxidizing the component in an oxygen containing environment at an elevated temperature, such as within a range of 950 to about 1300 degrees C, and more specifically in a range of about 1000 to about 1250 degrees C. Oxidation may be carried out in a dry or wet ambient, and is typically carried out at atmospheric pressure. A wet ambient can be generated by introducing steam, and functions to increase the rate of oxidation. The oxide layer is generally silicon oxide, typically SiO_2. The silicon oxide layer may be in direct contact with the silicon carbide of the component, as in the case of free-standing SiC or substrates coated with silicon carbide, such as by CVD.

[0026] The oxide layer may cause residual silicon carbide particulates to be converted to silicon oxide, in addition to formation of an oxide layer along the body proper. In the case of particulate conversion, oxidation may enable later stage particulate removal. In addition, formation of an oxide coating by a conversion process, rather than a deposition process, helps trap residual impurities, such as metallic impurities, within the oxide layer, for removal along with stripping of the oxide layer.

[0027] The oxide layer may be stripped by exposure of the processing component to a solution that is capable of solubilizing (dissolving) the oxide layer. In one embodiment, the solution is an acid which contains fluorine. Typically, the pH of the solution is less than about 3.5, most typically less than about 3.0, with some embodiments being even more acidic, having a pH less than about 2.5. Alternatively, the solution may be basic, and exposed to the layer in conjunction with elevated temperatures (greater than room temp, but below H2O boiling point). Alternatively, high temperature and H2 gas, such as above 1000 °C, may also be used.

[0028] During oxidation, the semiconductor processing component may be exposed to a reactive species, such as a halogen gas, that forms a reaction product with contaminants

present at the outer surface of the outer surface portion. Generally, both the exposure to a reactive species and oxidizing are carried out simultaneously, although alternatively the steps may be carried out separately. In this regard, use of the term simultaneously does not require that the exposure and oxidation steps to be carried out so as to be completely coextensive, but rather, the steps may overlap each other partially.

[0029] The term "halogen gas" denotes use of any halogen group elements provided in gaseous form, typically combined with a cation. An example of a common halogen gas which may be employed according to embodiments of the present invention includes HCl. Other gasses include those that contain fluorine, for example. Typically, the elevated temperature at which the semiconductor processing component is exposed to the halogen gas is sufficient to enable a reaction between the halogen gas and impurities contained along an outer surface portion of the semiconductor processing component, including along the exposed outer surface of the semiconductor processing component. For example, the elevated temperature may be within a range of about 950° C to about 1300° C. Further, the concentration of the halogen gas may vary, and may be present in the heated environment (e.g., a furnace processing chamber) within a range of about 0.01 to about 10% of the total pressure. Typically, the lower limit of the partial pressure is somewhat higher, such as about 0.05, or about 0.10%. While the foregoing has focused halogen gases, other reactive anion-containing reactants may be utilized, provided that the reactant is chosen so as to form a reaction product with expected metallic impurities, and that the reaction product has a higher volatility than that of the metallic impurity itself.

[0030] Typically, the impurity with which the halogen gas reacts along an outer surface portion of the semiconductor processing component is a metal impurity. Metal impurities may take on the form of elemental metal, or metal alloys, and may be aluminum-based, iron-based, or chromium-based, for example. The use of a halogen gas such as HCl causes the formation of a reaction product with such metal impurities. The reaction product typically has a higher volatilization than the impurities, such that during the exposure of the processing component to the elevated temperature, the reaction product volatilizes and is thus removed from the processing component.

[0031] While the above disclosure has focused on removal of a portion of the component by reacting, notably by oxidation-stripping, other techniques for removing the target portion may be utilized. For example, the target portion may be reacted by an etching operation, by introducing an etchant species at an elevated temperature to form an etchant product that volatilizes to wholly or partly remove the target portion. For example, the etchant species may be a chlorine-containing gas, forming $SiCl_x$ etchant product that volatilizes. The Cl-containing gas may be HCl, Cl_2, and others. In some cases, carbon may be left behind as a by-product of the etching operation. This carbon may be removed by a high temperature burn-out treatment. It is noted that sometimes etching is referred to as graphitization, describing the carbon in the form of graphite left behind on the surface of the component. It is also generally desirable that the etchant used complexes with the impurities present along the outer surface portion, forming volatilized species such as FeCl, TiCl, etc. Further, as described above, to the extent that oxidation and oxide stripping are utilized to remove the target portion, the contaminants may be reacted to form a reaction product, such as by introducing a halogen gas as already described above in detail.

[0032] Prior to removal of the target portion by any of the techniques disclosed herein, the component may be subjected to a machining operation, to remove, for example 10 to 100 microns of outer material of the component. While the as-deposited impurity profile is generally altered by material removal from machining operations, machining tends to nevertheless leave a spike in impurities at the outer surface of the component (i.e., the as-machined surface), as similarly observed in as-deposited CVD SiC. It has been found that the surface impurity level may extend into the outer surface portion, such as on the order of 1-3 microns, before reaching the bulk impurity level. Accordingly, in embodiments that have been subjected to machining, oftentimes the target portion to be removed has a thickness at the higher end of the above noted range of up to about 20 microns, with actual thicknesses removed on the order of 3 to 5 microns. Accordingly, to the extent that the CVD-SiC surface of the component is subjected to a mechanical abrasion or machining process such as grinding, lapping or polishing, prior to removal of the target portion, further removal would generally be effected due to elevated

contamination levels present in the post-machined surface. Removal of the target portion may executed with oxidation-strip cycles or etching cycles, for example, carried out enough times to effect high purity.

[0033] According to another feature, removal of the target portion is carried out prior to use of the processing component in a semiconductor fabrication environment. As such, the foregoing steps may be carried out off-site, separate from the semiconductor fabrication environment, such as by the manufacturer of the processing component rather than the end user (e.g., the semiconductor component manufacturer/wafer processor). The processing component may be fully treated, then packaged in a hermetic shipping container for direct and immediate use in a fabrication environment. While the foregoing has focused on one cycle, processing steps such as oxidation-steps (with optional halogen gas treatment) may be repeated, and is generally repeated, several times to achieve the desired level of purity through removal of the target portion.

[0034] According to a variant, additional processing steps may be incorporated prior to target portion removal, with an aim to further reduce impurity levels. For example, the component may be rinsed, such as with deionized (DI) water, prior to exposure to halogen gas and subsequent processing. Agitation may be carried out during rinsing, such as with an ultrasonic mixer/agitator, to further supplement contaminant removal. Further, the rinsing solution may be acidic solution to aid in stripping the contaminants.

[0035] Alternatively, or in addition to rinsing, the component may be immersed in an acidic stripping solution prior to halogen species exposure, such as an acidic solution, to further aid in impurity removal. The rinsing and/or immersion steps may be repeated any number of times prior to further processing.

[0036] Due to the observed depth profiling as described in more detail below, typically the target portion has a thickness of at least about 0.25 microns, such as 0.38 microns, 0.50 microns, and even higher. Indeed, the target portion most generally has a thickness of at least 1.0 microns, and preferably at least about 2, such as about 2-10 microns microns, but generally less than 20 microns. Typically the CVD-SiC layer has a thickness with a range of about 10 to 1000 μm, and certain embodiments have a thickness

up to about 800 μm, 600 μm, 400 μm, or up to about 200 μm. The thickness of the target portion corresponding to the depth of removal of the outer surface portion of the component is generally chosen to ensure the desired surface impurity reduction, such as driving the impurity content down from 1,000 X of bulk to on the order of 10 X of bulk, or even lower. Indeed, the surface impurity level is generally reduced by at least one order of magnitude if not two orders of magnitude as a result of the removal of the target portion.

[0037] With respect to the particular measurement techniques for characterizing pre- and post-treated CVD-SiC films, particular use is made of Secondary Ion Mass Spectroscopy (SIMS). Other techniques include GDMS, for example. As used herein, the bulk impurity level generally corresponds to the impurity level at a depth within the outer surface portion at which the purity level is stabilized, that is, is generally constant further into the depth of the outer surface portion. It is noted that impurity detection usually entails some degree of variance, represented by swings in measured impurity levels as a function of depth. Unless otherwise noted herein, while raw data is reported, specific impurity level data points, and particularly the bulk impurity level, are based upon a trend of the impurity contents according to the data, that is, smoothed data. According to characterization studies reported herein, it was found that typically the bulk impurity level is typically reached by a depth of 3 microns. Accordingly, the bulk impurity level may be taken at a depth within a range of about 3 to 10 μm, such as within a range of 3 to 5 μm, for example. The particular depth value at which the bulk impurity level is reached, however, may be dependent on processing conditions of the particular CVD process utilized to form the outer surface portion, including particular tool used, gases used, temperature, pressure, and other processing parameters.

[0038] According to a particular embodiment, the bulk impurity level is not greater than about 1e17 atoms/cc iron (Fe) and not greater than 1e15 atoms/cc chromium (Cr). Of course, more demanding end use applications of processing components may call for even lower bulk impurity levels than the foregoing, such as 1e16 atoms/cc iron (Fe).

[0039] The data and following discussion focus on characterization studies done on several as-deposited CVD-SiC samples as well as on post-treated CVD-SiC samples.

[0040] Si:SiC coupons of size 25 mm x 75 mm x 6 mm were prepared using standard processing. The coupons were ultrasonically cleaned in dilute acid, DI water rinsed, and dried. The cleaned coupons were loaded into the CVD reactor and a CVD film between 12-18 microns in thickness was deposited on the surface of the Si:SiC coupons. Multiple coating runs were performed using two different coating systems (Apparatus A and Apparatus B) to further understand equipment effects on coating purity.

[0041] The impurity level on the surface of the CVD coated Si:SiC coupons was analyzed by Secondary Ion Mass Spectroscopy (SIMS). The SIMS analysis was conducted with O_2^+ plasma using a Cameca 3f instrument in a depth profile mode. The instrument was calibrated using ion implanted SiC standards for accurate impurity determination. The analysis was focused on Fe and Cr alone to enable a good detection limit, viz. 1e15 atoms/cc for Fe and 1e14 atoms/cc for Cr. Unless otherwise noted, the results described hereinafter represent as-deposited or as-removed CVD-SiC, with no intermediate machining operations.

[0042] The SIMS analysis of the CVD-SiC layer of a sample processed by Apparatus A, indicates a high surface contamination of both Fe and Cr that is 500-1000 times higher than the bulk value as shown in FIG. 2. The Fe concentration in the bulk is <1e15 atoms/cc and the Cr concentration is <1e14 atoms/cc, which is typical for CVD-SiC coatings.

[0043] A similar high surface impurity concentration was also observed on the CVD-SiC layer deposited using Apparatus B, as shown in FIG. 3.

[0044] The surface Fe concentration is >1e18 atoms/cc and drops to the bulk value of <1e15 atoms/cc within 0.5 microns depth into the CVD-SiC coating for the particular samples under characterization. To verify the universality of high impurity concentration on the surface of as-deposited coatings, a third test was conducted on a CVD-SiC coating with higher impurities in the reactant gases used to form the CVD film. Impurity

enrichment was also observed on coatings with higher impurity levels as shown in FIG. 4. The Fe concentration at the surface is >1e19 atoms/cc, and drops over 2-2.5 microns to the bulk Fe concentration of 5 e16 atoms/cc. The Cr at the surface is 5e17 atoms/cc, which is a factor of 550 higher than the bulk Cr concentration of 7e14 atoms/cc. The relatively gradual drop in impurity concentration from the surface to the bulk may be related to differences in surface roughness between the coatings under characterization.

[0045] Mechanisms for impurity enrichment at the surface are not well understood at the present but may relate to impurity migration from the surface of the Si:SiC substrate during the CVD-SiC deposition process or Fe segregation from the interior of the film to the surface during cooling.

[0046] Two different types of CVD-SiC coatings were produced with Apparatus A, a standard coating and a lower-purity coating, were selected for cleaning processing. The coupons were loaded onto a CVD coated cantilever paddle and placed into a diffusion furnace equipped with a SiC process tube.

[0047] The coupons were oxidized at 950-1350°C for 6-14 hours in flowing O2 with up to 10% HCl gas. The thermal treatment conditions were selected to enable the growth of a thick thermal oxide on the CVD-SiC surface through consumption of a target portion of the CVD-SiC corresponding to about 0.45-0.60, nominally 0.5 times the thickness of the oxide. The oxidation process helps to concentrate the transition metal impurities such as Fe into the oxide layer on the CVD-SiC. While the HCl gas helps to volatilize the impurities on the surface of the growing oxide, HCl treatment is not believed to significantly remove metal trapped within the growing oxide layer. The overall process consumes the contaminated target portion of the CVD-SiC layer through the reaction, $SiC + 3/2\ O2\ (g) = SiO2 + CO(g)$ to form SiO2.

[0048] To remove the bulk impurities within the oxide layer, the oxide layer was stripped in an acid bath using a HF-HCl mixture (1:1 acid mixture). The resulting impurity concentration at the surface is shown in FIG. 5.

[0049] SIMS analysis indicates that the surface Fe concentration decreases from >5e17 atoms/cc on the initial CVD-SiC coupon to <5e16 atoms/cc on the cleaned coupon, a 10 fold improvement due to cleaning. The bulk impurity concentration remained constant at <1e15 atoms/cc. While the cleaning cycle decreased surface impurity concentration, the surface impurity concentration was still a factor of 50 higher than the bulk. Thus, an additional cleaning cycle was conducted to further decrease the Fe concentration at the surface. The effect of the 2^{nd} cleaning cycle could not be quantified using SIMS due to detection limit issues and noise in the analysis. Accordingly the cleaning cycles were repeated using the CVD-SiC sample with higher impurities (shown in FIG. 4) to help discern minor differences between the surface and bulk impurity levels.

[0050] The lower purity CVD-SiC sample was cleaned similar to the standard CVD-SiC sample. The coupons were first oxidized at 950-1350°C for 6-14 hours in flowing O2 with up to 10% HCl gas to grow an oxide layer that was subsequently stripped by the HF-HCl solution. The cleaning cycle was repeated a second time to remove material deeper into the CVD-SiC surface and thereby remove the Fe-enriched surface layer.

[0051] SIMS analysis of coupons after two cleaning cycles is shown in FIG. 6. The double cleaning cycle was effective to completely remove the contaminated surface layer, and the surface impurity concentration is similar to the bulk impurity concentration.

[0052] It is again noted that, while the foregoing characterization studies have taken advantage of repeated oxidation-strip cycles coupled with halogen gas treatment, other removal techniques may be employed for removal of the target portion. Further, it has been found that repeated removal steps may be carried out in order to drive the surface impurity levels to a desirable range as described above, a single cycle resulted in a surface impurity level that was dramatically improved, but still having an impurity level that was 50 X that of the bulk. Accordingly, repeated cycles are generally carried out to ensure bulk-like purity at the surface.

[0053] Still further, as demonstrated by FIG. 6, the techniques described herein may be carried out to reduce the impurity level of the surface to be not greater than the bulk impurity level, that is, about equal to or less than the bulk impurity level. Note that the

data shown in FIG. 6 were taken from two different samples, and are provided for comparative purposes to show impurity trends before and after treatment. .

[0054] The above-disclosed subject matter is to be construed as illustrative and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments that fall within the scope of the present invention. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents and shall not be restricted or limited by the foregoing detailed description.